Application No.: 10/716,615

Amendments to the Specification

Please add the following paragraph subsequently to the paragraph on page 7, line 14:

FIG. 7 is a circuit diagram of a modified receiver circuit according to Embodiment 1 of the invention.

Please replace the paragraph on page 10, line 22 to page 11, line 3 with the following amended paragraph:

Also, in this embodiment, the reset signal to be output to the data processing unit 100 is controlled on the basis of the number of transitions of the signal detected in the signal detection unit 300, so as to restrict (control to reset) the operation of the data processing unit 100. In the case where the data processing unit 100 has a power down signal input terminal NPD (the input buffer 1 and the serial-parallel converter circuit 2 each have the power down signal input terminal NPD), the output signal from the signal detection unit 300 can be input as a power down signal to the power down signal input terminal NPD so as to power-down control the operation of the data processing unit 100, as shown in Fig. 7.

Please replace the paragraph on page 12, lines 16-21 with the following amended paragraph:

Also in this embodiment, the operation for resetting the data processing unit 100 is controlled on the basis of the number of transitions of the output signal RSIG of the offset buffer 6 occurring in the predetermined time in the signal detection unit 400. Instead, in the case where the data processing unit 100 has a power down signal input terminal, a power down signal can be

Application No.: 10/716,615

input to this power down signal input terminal, so as to power-down control the data processing unit **100** (see Fig. 7).

Please replace the paragraph on page 14, lines 1-9 with the following amended paragraph:

In this embodiment, the reset signal NRESET is output to the data processing unit 100 when the number of transitions occurring in the predetermined time of the output signal RSIG of the offset buffer 6 of the signal detection unit 500 detected by the frequency detection circuit 5 is not more than the given set value, so as to control to reset the operation of the data processing unit 100. Instead, in the same manner as described in Embodiments 1 and 2, in the case where the data processing unit 100 has a power down signal input terminal, a power down signal can be used as the signal from the frequency detection circuit 5 to the data processing unit 100, so as to power-down control the operation of the data processing unit 100 (see Fig. 7).

Please replace the paragraph on page 15, lines 4-8 with the following amended paragraph:

Also in this embodiment, in the same manner as described in Embodiments 1 through 3, in the case where the data processing unit **100** has a power down signal input terminal, a power down signal can be output as the output signal of the frequency detection circuit **5** instead of the reset signal, so as to control the operation of the data processing unit **100** (see Fig. 7).